
Training Catalog



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About Us

AvionChip Technology Inc. was founded by Dr. Vecdi Emre Levent in 2022 at the Bogazici University Technopark (BUDOTEK)

Main services are:

- Developing IP cores for FPGAs
- Embedded Systems
- FPGA training and consultancy

Training Contents

The training services provided are listed in categories below. Details of the training content are on the following pages.

HDL & HLS & Libraries

- Fundamentals of Digital Design
- Verilog Comprehensive
- System Verilog for Validation
- System Verilog for Design
- UVM
- HLS Tools

Design Environments

- Xilinx Vivado & Vitis Design Environment
- Intel Quartus Design Environment
- Lattice Diamond Design Environment
- Microsemi Libero Design Environment
- Efinix Efinity Design Environment
- Gowin EDA Design Environment

Interfaces

- PCI Express
- Ethernet
- USB
- Transceivers
- High Speed Memory
- Low Speed Interfaces

Design Methodologies

- Clock Domain Crossing
- Pipelining & Resource Sharing
- Basic Validation Procedures
- Security Critical Designs
- Partial Reconfiguration
- DSP IPs
- Xilinx Based IPs for Video Processing

Embedded Linux

- Linux Basics
- Petalinux
- Petalinux for Video Processing
- Ubuntu FS

Xilinx FPGA Architectures

- Artix 7 & Kintex 7 Architectures
- ZYNQ 7000 Architecture
- Ultrascale+ Architecture
- MPSOC Architecture
- RFSOC Architecture
- Versal Architecture
- Python Development Environment for ZYNQ Architecture
- Deep Learning
- Xilinx High Level Synthesis
- Xilinx XRT
- Vitis Vision Library
- Vitis AI Library
- Vitis OpenCV
- Vitis Blas
- Vitis Fintech

Intel FPGA Advanced Architect

- IntelCyclone Architecture
- Intel SOC Architecture
- Arria 10 Architecture
- OpenCL Synthesis

Programming and Scripting Languages

- C
- C++
- Python
- Perl
- Linux Bash Scripting
- TCL

Cloud-Based Development

- Xilinx Amazon AWS

Matlab Based Development

- HDL Coder
- Model Composer

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Comprehensive Verilog

Training Period:

- 4 Days

Training Content:

- Combinatorial Logic
- Sequential Logic
- State Machines
- Bus Elements
- Memories
- Optimizations and Tradeoffs

Software and Hardware to be used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

System Verilog for Verification

Training Period:

- 3 Days

Training Content:

- Data Types
- Interfaces
- Always Comb, Latch, FF Blocks
- Assertions
- Clocking Blocks
- Coverage
- Arrays and Queues
- DPI
- Class
- Inheritance
- Polymorphism
- Functional coverage

Software and Hardware to be Used:

- Vivado ML 2022.2
- QuestaSim
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system
- Verilog basics

System Verilog for Design

Training Period:

- 2 Days

Training Content:

- Data types
- Always Blocks
- User-defined types
- Interfaces
- Packages

Software and Hardware to be Used:

- Vivado ML 2022.2
- Synopsys Synplify
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system
- Verilog basics

UVM (Universal Verification Methodology)

Training Period:

- 3 Days

Training Content:

- Data modeling
- UVM Classes
- Factory Grade
- Transaction Level Modeling (TLM)
- Register Modeling

Software and Hardware to be Used:

- Vivado ML 2022.2
- Questasim
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system
- Verilog and System Verilog information

HLS Tools

Training Period:

- 1 Day

Training Content:

- Popular HLS tools other than Xilinx's HLS

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system
- Verilog information

Xilinx Vivado & Vitis Design Environment

Training Period:

- 4 Days

Training Content:

- Project operations
- Synthesis analyses
- I/O Planning
- Vivado IPs
- Design with IP Integrator
- Create an IP
- IP Packaging
- IP Security
- IP Usage
- AXI Interfaces
- Interconnect, SmartConnect
- Vivado Reports
- Microblaze
- Vitis Environment

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system
- Basic knowledge of RTL

Intel Quartus Design Environment

Training Period:

- 3 Days

Training Content:

- Design flow
- Pin assignments
- Constraints
- QSYS
- Signal Tab II

Software and Hardware to be Used:

- Quartus 2022.1
- Intel Cyclone 5

Required Skills

- Basic knowledge of the digital system

Lattice Diamond Design Environment

Training Period:

- 1 Day

Training Content:

- Design flow

Software and Hardware to be Used:

- Lattice Diamond
- iCE40UP iCE40 UltraPlus™

Required Skills

- Basic knowledge of the digital system
- RTL Basic Knowledge

Microsemi Libero Design Environment

Training Period:

- 1 Day

Training Content:

- Design flow

Software and Hardware to be Used:

- Microsemi Libero
- AGLN-NANO-KIT

Required Skills

- Basic knowledge of the digital system
- Basic knowledge of RTL

Efinix Efinity Design Environment

Training Period:

- 4 Days

Training Content:

- Design flow

Software and Hardware to be Used:

- Efinix Efinity
- Trion T20

Required Skills

- Basic knowledge of the digital system
- RTL Basic Knowledge

Gowin EDA Design Environment

Training Period:

- 1 Day

Training Content:

- Design Flow

Software and Hardware to be Used:

- Gowin EDA
- DK-START-GW1NSR

Required Skills

- Basic knowledge of the digital system
- RTL basic knowledge

PCI Express

Training Period:

- 1 Day

Training Content:

- XDMA
- Creating an XDMA Reference Design
- PCIE Driver and User Software
- Windows/Linux Drivers
- Recommendations for High Performance
- Interrupt vs Polling Mode

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Ultrascale+

Required Skills

- Basic knowledge of the digital system

Ethernet

Training Period:

- 2 Days

Training Content:

- OSI Layers
- PHY Interfaces
- PHY Chips
- TEMAC IP
- Protocols
 - UDP
 - TCP
 - DHCP
 - HARP
- Host Software Development
- 10/25G Ethernet IPs
- Microblaze Based Ethernet

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

USB

Training Period:

- 1 Day

Training Content:

- USB Data Transfers
- Host Software Development

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Transceiver

Training Period:

- 2 Days

Training Content:

- PMA
- PCS
- Reference Clock vs PLLs
- Equalization
- Transmit De-Emphasis
- Receiver Equalization
- IBERT
- Line Settings
- Transceiver Selection
- Clocking Settings
- Design with Silicon Labs Programmable Oscillator
- Physical Resources
- Reference Design Creation
- Simulating the Reference Design
- Channel Bonding
- Channel Bonding Simulation

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

High Speed Memory

Training Period:

- 1 Day

Training Content:

- MIG(Memory Interface Generator)
- Mode and Interface
- Clocking
- Controller Settings
- Memory Settings

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Low Speed Interfaces

Training Period:

- 1 Day

Training Content:

- UART
- SPI
- I2C
- Logic and Processor Based

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Clock Domain Crossing

Training Period:

- 1 Day

Training Content:

- Metastability
- Synchronization
- Design with Multi Clock

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Pipelining & Resource Sharing

Training Period:

- 1 Day

Training Content:

- Frequency Amplification Techniques
- Pipelining Techniques
- Space Utilization Reducing Common Use

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Basic Validation Procedures

Training Period:

- 2 Days

Training Content:

- Verification Methodology
- Testbench Preparation
- Black Box vs White Box
- Fork-Join
- Automated TestBench Preparation
- Observation Functions
- Loops
- Task and Functions
- File operations
- In-Chip Verification
- JTAG to AXI Master
- ILA (Integrated Logic Analyser)
- System ILA
- VIO
- Image Verification IPs

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Security Critical Designs

Training Period:

- 1 Day

Training Content:

- Verilog Best-Practices
- Code Coverage
- TMR (Triple Modular Redundancy)
- ECC (Error Correction Checking)
- CRC (Cyclic Redundancy Checking)
- Safe State Machines

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Partial Reconfiguration

Training Period:

- 1 Day

Training Content:

- Partial Reconfiguration Requirements
- PBlocks
- Partial Reconfiguration over PCIe

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

DSP IPs

Training Period:

- 1 Day

Training Content:

- CORDIC
- FFT
- DFT
- Complex Multiplier
- Floating Point
- DDS Compiler
- Adder/Subtractor
- FIR

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Xilinx Based IPs for Video Processing

Training Period:

- 1 Day

Training Content:

- VDMA
- VPSS
- Video Scaler

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Linux Basics

Training Period:

- 1 Day

Training Content:

- Basic Linux Commands
- Introduction to Bash Scripting

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Petalinux

Training Period:

- 3 Days

Training Content:

- Petalinux ToolChain
- Kernel
- U-Boot
- FileSystem
- Application Development
- PL/PS CoProcessing

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx ZYNQ 7000

Required Skills

- Basic knowledge of the digital system

Petalinux for Video Processing

Training Period:

- 1 Day

Training Content:

- PL/PS Video Transfer Techniques

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx ZYNQ 7000

Required Skills

- Basic knowledge of the digital system

Ubuntu FS (File System)

Training Period:

- 1 Day

Training Content:

- Petalinux with Ubuntu FileSystem

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Artix 7 & Kintex 7 architectural design

Training Period:

- 1 Day

Training Content:

- CLB
- MMCM
- PLL
- I/O Clocking
- Drives
- DSPs

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

ZYNQ 7000 Architecture

Training Period:

- 3 Days

Training Content:

- PS Blocks
- Interfaces
- Baremetal Applications
- PL/PS Communication
- AXI Interfaces

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Ultrascale+ Architecture

Training Period:

- 1 Day

Training Content:

- Drives
- RTL UltraRAM
- XPM UltraRAM
- Device Primitives
- CLB
- DSP
- IO SERDES

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Ultrascale+

Required Skills

- Basic knowledge of the digital system

MPSOC Architecture

Training Period:

- 3 Days

Training Content:

- Architecture
- APU
- Real-Time CPU
- H264/265 CODEC UNIT
- MALI GPU

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx MPSOC

Required Skills

- Basic knowledge of the digital system

RFSOC Architecture

Training Period:

- 1 Day

Training Content:

- Real-Time CPU
- DAC/ADC

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx RFSOC

Required Skills

- Basic knowledge of the digital system

Versal Architecture

Training Period:

- 2 Days

Training Content:

- Embedded AI Blocks
- Machine Learning Applications

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Python Development Environment for ZYNQ Architecture

Training Period:

- 1 Day

Training Content:

- Python-based development methodology

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Deep Learning

Training Period:

- 1 Day

Training Content:

- AI development methodology with Xilinx DPU

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Xilinx High Level Synthesis

Training Period:

- 2 Days

Training Content:

- Vitis HLS
- Types of I/O
- Latency Reduction
- Space Usage Improvement

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Xilinx XRT

Training Period:

- 1 Day

Training Content:

- Xilinx Runtime Environment

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Xilinx Vision Library

Training Period:

- 1 Day

Training Content:

- Image processing HLS Library

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Vitis AI Library

Training Period:

- 1 Day

Training Content:

- AI Library

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Vitis OpenCV

Training Period:

- 1 Day

Training Content:

- Xilinx Video Processing OpenCV Library

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Vitis BLAS

Training Period:

- 1 Day

Training Content:

- Library of linear Algebra operations

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Vitis Fintech

Training Period:

- 1 Day

Training Content:

- HLS Library of Financial Technologies

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Intel Cyclone Architecture

Training Period:

- 1 Day

Training Content:

- Intel Cyclone Architecture

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Intel SOC Architecture

Training Period:

- 1 Day

Training Content:

- ARM A9 Architecture
- SOC PL/PS Architecture

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Intel Arria 10 Architecture

Training Period:

- 1 Day

Training Content:

- Arria 10 Architecture
- Embedded FPU

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Intel FPGA OpenCL Synthesis

Training Period:

- 1 Day

Training Content:

- OpenCL Synthesis to SOC Platforms

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

C Language

Training Period:

- 3 Days

Training Content:

- Basic C Language Teaching

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

C++ Language

Training Period:

- 3 Days

Training Content:

- C++ with Object-Oriented Programming Concept

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Python

Training Period:

- 4 Days

Training Content:

- Basic and Advanced
- Object Oriented

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Perl

Training Period:

- 1 Day

Training Content:

- Basic Perl Script Development

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Linux Bash Scripting

Training Period:

- 1 Day

Training Content:

- Bash Scripting

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

TCL

Training Period:

- 1 Day

Training Content:

- Script Development in the Vivado TCL Environment

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

Xilinx Amazon AWS

Training Period:

- 1 Day

Training Content:

- Developing with Amazon Servers Infrastructure

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

MATLAB HDL Coder

Training Period:

- 1 Day

Training Content:

- RTL Production with Matlab HDL Coder Tool

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system

MATLAB Model Composer

Training Period:

- 1 Day

Training Content:

- RTL Generation with Matlab Model Composer Tool

Software and Hardware to be Used:

- Vivado ML 2022.2
- Xilinx Artix 7

Required Skills

- Basic knowledge of the digital system